transistor of the first type by its source and its drain, respectively. The capacitor has a first terminal directly connected to the first supply terminal and a second terminal directly connected to the gate so the MOS transistors of the second type.

Fig. 5 of Merrill illustrates a circuit for protecting and an integrated circuit from damage caused by an electrostatic discharge. As described in column 4, lines 63 - 68 of Merrill, a voltage spike on the terminal VCC turns on the field effect transistor (FET) 42 via the capacitor 40 so as to short the terminal VCC to ground via FET 42. For FET 42 to turn on in this situation, it must be an n-channel FET so that a positive voltage at its gate will cause it to become conductive.

FET 43, on the other hand, is intended to pull down the gate of FET 42 (to prevent FET 42 from becoming conductive) when a normal operating voltage is present between VCC and ground. The time constant of the (resistor-capacitor) RC circuit including resistor 45 and capacitor 47 is set to be greater than the time period of a typical electrostatic discharge event. Therefore, if a brief voltage spike (e.g., an electrostatic discharge) appears at the node VCC at a time when a normal operating voltage is not applied between VCC and ground, the gate of the FET 43 (i.e., the node between the resistor 45 and the capacitor 47) will not rise to a level sufficient to turn on the FET 43. However, the same brief voltage spike will cause the gate of FET 42 to rise to a level sufficient to turn it on and short VCC to ground during the time period of the discharge event.

If a voltage remains on node VCC for a period of time in excess of the RC time constant of the resistor 45 and the capacitor 47 (e.g. during normal power application to the circuit), the voltage at the gate of the FET 43 will rise to, and will remain at, the voltage VCC so as to hold the gate of the FET 42 at ground. To perform this function, FET 43 must also be an n-channel FET so that a positive voltage at its gate will cause it to become conductive.

Therefore, each of FETs 42 and 43 in Fig. 5 of Merrill clearly are of the same type (i.e., n-channel), and Merrill does not disclose or suggest the claimed invention including MOS transistors of two different types.

Claim 1 therefore distinguishes over Merrill, and the rejection of this claim under 35 U.S.C. §103(a) as being unpatentable over Merrill should be withdrawn. Each of the claims

2, 4, 5, and 27-33, being dependent on claim 1, should be allowable for at least the same reasons.

Claims 3 and 6

Claim 3 was objected to as being dependent on a rejected base claim, but was indicated as being allowable if rewritten in independent form to include the limitations to the base claim and any intervening claims. Applicant has so amended claim 3. Claim 3 therefore should be in allowable condition. Claim 6, being dependent on claim 3, should be allowable for at least the same reasons.

Claim 18-22 and 34-37

Claims 18-22 and 34-39 have been allowed.

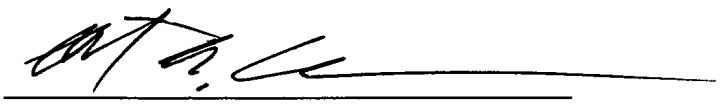
CONCLUSION

Applicant believes that this application now is in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this Amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

Serge Pontarollo,



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